Claims

[1] An apparatus for generating clock pulses using a Direct Digital Synthesizer (DDS), the apparatus comprising:

a DDS comprising:

a Phase Locked Loop (PLL) multiplier for receiving system reference clock pulses of a first frequency and converting the system reference clock pulses into a DDS operation clock signals of a second frequency;

a phase accumulator for receiving a Frequency Tuning Word (FTW), accumulating a phase by the FTW and outputting the phase of a desired particular frequency, wherein the phase accumulator operates using the DDS operation clock signals from the PLL multiplier;

a phase-to-magnitude for, in responsive to the accumulated phase of the particular frequency from the phase accumulator, providing a clock signal having a magnitude corresponding to the phase of the particular frequency, wherein the phase-to-magnitude operates using the DDS operation clock signals from the PLL multiplier;

a Digital-to-Analog (DA) converter for, in responsive to the clock signal from the phase-magnitude converter, converting the clock signal to an analog signal of a DDS output frequency, wherein the DA converter operates using the DDS operation clock signals from the PLL multiplier;

a band pass filter for bandpass-filtering the analog signal of the DDS output frequency from the DA converter to provide a bandpass-filtered signal; and

a comparator for, in responsive to the bandpass-filtered signal from the band pass filter, transforming the signal of the DDS output frequency into a square wave.

[2] The apparatus of Claim 1, wherein the Phase Locked Loop (PLL) multiplier is a 10X PLL multiplier, and wherein the first frequency of the system reference clock pulses is 19.6608 MHz and the second frequency of the DDS operation clock signals is 196.608 MHz.

[3] The apparatus of Claim 1, wherein the FTW is derived from equations (1) and (2) below.

$$f_{out} = (W * f_{clk})/2^N \quad (1)$$

$$W = INT[(f_{out}/f_{clk})*2^N] \quad (2)$$

where f_{out} is a DDS output frequency, W is a binary value for the FTW, f_{clk} is a DDS operation clock frequency, N is the number of input bits of the phase ac-

cumulator, and INT[] denotes an integer part of the bracketed expression.

[4] The apparatus of Claim 1, wherein the square wave has a low jitter.